CLAIMS:

Having thus described our invention, what we claim as new and desire to secure by Letters Patent is as follows:

1. In an interconnection structure suitable for flip-chip attachment of microelectronic device chips to chip carriers, a three-layer ball limiting metallurgy comprising:

an adhesion layer for deposition on a wafer or substrate;

a solder reaction barrier layer of a material selected from the group consisting of Ti, TiN, Ta, TaN, Zr, ZrN, V and Ni; and

a solder wettable layer.

2. The interconnection structure of claim 1, wherein the adhesion layer is formed of a material selected from the group consisting of Cr, TiW, TiN, TaN, Ti, Ta, Zr, and ZrN.

3. The interconnection structure of claim 1, wherein the solder wettable layer is formed of a material selected from the group consisting of Cu, Pd, Co, Ni, Au, Pt, and Sn.

4. The interconnection structure of claim 1, further comprising an optional fourth layer is formed

of a material selected from the group consisting of Au and Sn, if Au or Sn is not used in the third layer.

5. The interconnection structure of claim 1, wherein said adhesion layer is comprised of one of Cr and TiW, said reaction barrier is comprised of Ti, and said solder wettable layer is comprised of one of Cu, Co, Ni, Pd and Pt.

6. An interconnection structure suitable for flip-chip attachment of microelectronic device chips to packages, comprising:

a two-layer ball-limiting composition comprising an adhesion/reaction barrier layer, wherein the adhesion/reaction barrier layer serves both as an adhesion and reaction barrier layer, and a solder wettable layer, said adhesion/barrier layer being for placement between a microelectronic device and said solder wettable layer, and wherein said solder wettable layer is of a metal reactive with components of a tin-containing lead-free solder, so that said solder wettable layer is consumed during soldering, wherein the adhesion/reaction barrier layer remains after being placed in contact with said lead free solder during soldering; and

one or more lead=free solder balls selectively situated on said solder wettable layer, said lead-free solder balls comprising tin as a predominant component and one or more alloying components.

7. The interconnection structure defined in claim 6, wherein said adhesion/reaction barrier layer is comprised of a material selected from the group consisting of Ti, TiN, TiW, Ta, TaN, Zr, ZrN and V.

8. The interconnection structure defined in claim 6, wherein said solder wetting layer is comprised of a material selected from the group consisting of Cu, Ni, Co, Pd, Pt, Au and Sn.

9. The interconnection structure defined in claim 6, ~~further comprising an optional third layer comprised of~~ Au or Sn, ~~if the second layer is not formed of Au or Sn.~~

~~10. The interconnection structure defined in claim~~ 6, wherein said lead-free solder ball is comprised of a ~~material that substantially avoids alpha particle~~ emission.

11. The interconnection structure defined in claim ~~6, wherein said alloying components are selected from~~ the group consisting of Sn, Bi, Cu, Ag, Zn and Sb.

12. The interconnection structure defined in claim ~~6, adhesion/reaction barrier layer comprises Ti and~~ said solderable layer comprises one of Cu, Co, Ni, Pd ~~and Pt.~~

13. An interconnection structure suitable for flip-chip attachment of microelectronic device chips to packages, comprising:

a three-layer ball-limiting composition comprising an adhesion layer, a reaction barrier layer on top of said adhesion layer and a solder wettable layer, wherein said adhesion/barrier layer is between a microelectronic device and said solder wettable layer and wherein said solder wettable layer is of a composition sufficiently reactive with components of a tin-containing lead free solder, and the reaction barrier layer is substantially less-reactive with solder after being placed in contact therewith in a solder joining process; and

one or more lead-free solder balls selectively situated on said solder wettable layer, said lead-free solder balls having tin as a predominant component and one or more alloying components selected from the group consisting of Cu, Zn, Ag, Bi and Sb, whereby said lead-free solder ball substantially avoids alpha particle emission and induced soft logic errors which result therefrom.

14. The interconnection structure defined in claim 13, wherein said solderable layer is formed of a material selected from the group consisting of Cu, Ni, Co, Pd, PdNi, PdCo, NiCo, Au, Pt and Sn.

15. A method for forming an interconnection structure suitable for flip-chip attachment of microelectronic device chips to packages, comprising:

forming a ball limiting composition on a substrate;

forming a resist pattern on the ball limiting composition;

etching the ball limiting composition by using the resist as an etch mask;

removing the resist from remaining ball limiting composition; and

depositing solder on the ball limiting composition.

16. A method as recited in claim 15, wherein the solder is substantially lead free.

17. A method as recited in claim 15, wherein the ball limiting composition is formed by:

depositing an adhesion layer on said substrate;

depositing a reaction barrier layer on said adhesion layer; and

depositing a solder wettable layer on said barrier layer.

18. A method as recited in claim 17, wherein said reaction barrier layer is comprised of a material selected from the group consisting of Ti, TiN, Ta, TaN, Zr, ZnN, V and Ni.

19. A method as recited in claim 17, wherein said adhesion layer is deposited by sputtering, plating or evaporating.

20. A method as recited in claim 17, wherein said adhesion layer is deposited so as to have a thickness of about 100 to about 4000 Angstroms.

21. A method as recited in claim 17, wherein said reaction barrier layer is deposited by sputtering, plating or evaporation.

22. A method as recited in claim 21, wherein said reaction barrier layer is deposited so as to have a thickness of about 100 to about 20,000 angstroms.

23. A method as recited in claim 17, wherein said solder wettable layer is deposited by sputtering, plating or evaporation.

24. A method as recited in claim 17, wherein said solder wettable layer is deposited so as to have a thickness of about 100 to about 20,000 angstroms.

25. A method as recited in claim 17, further comprising depositing a layer comprising Au or Sn on said solder wettable layer.

26. A method as recited in claim 25, wherein the layer deposited on said solder wettable layer has a

thickness of between substantially 100 to substantially 20,000 angstroms.

27. A method as recited in claim 25, wherein the layer deposited on said solder wettable layer is deposited by one of sputtering, electro- or electroless plating or evaporation.

28. A method as recited in claim 15, wherein the ball limiting composition is formed by:

depositing an adhesion/reaction barrier layer on said substrate; and

depositing a solder wettable layer on said barrier layer.

29. A method as recited in claim 15, further comprising annealing the ball limiting composition at 150 - 250 degrees C for 30 to 60 minutes.

30. A method for forming an interconnection structure suitable for flip-chip attachment of microelectronic device chips to chip carriers, comprising:

depositing an adhesion layer on a wafer or substrate serving as said chip carrier;

depositing a solder reaction barrier layer on said adhesion layer;

depositing a solder wettable layer on said reaction barrier layer;

depositing a lead free solder on said solder wettable layer; and

reflowing said solder so that said solder wettable layer diffuses into said lead free solder.

31. A method as recited in claim 30, wherein said solder wettable layer contains Cu, and said Cu diffuses into said solder.

32. A method as recited in claim 31, wherein said lead free solder is substantially pure Sn, and a binary Sn-Cu lead-free solder is formed during reflowing.

33. A method as recited in claim 31, wherein said lead free solder is substantially binary Sn-Ag, and a ternary Sn-Ag-Cu lead-free solder is formed during reflowing.

34. A method as recited in claim 33, wherein a eutectic solder is formed.

35. A method as recited in claim 30, wherein a number of elements in said solder is increased by at least one element, by said diffusion.

36. A method as recited in claim 30, further comprising annealing at 150 - 250 degrees C for 30 to 60 minutes.

37. A method for forming an interconnection structure suitable for flip=chip attachment of microelectronic device chips to chip carriers, comprising:

depositing an adhesion layer on a wafer or substrate serving as said chip carrier;

depositing a solder reaction barrier layer which is solder wettable on said adhesion layer;

depositing a lead free solder on said solder wettable layer; and

reflowing said solder so that said solder wettable layer diffuses into said lead free solder.

38. A method as recited in claim 37, wherein said solder wettable layer contains Cu, and said Cu dissolves into said solder.

39. A method as recited in claim 38, wherein said lead free solder is substantially pure Sn, and a binary Sn-Cu lead-free solder is formed during reflowing.

40. A method as recited in claim 38, wherein said lead free solder is substantially pure Sn-Ag, and a ternary Sn-Ag-Cu lead-free solder is formed during reflowing.

41. A method as recited in claim 40, wherein a eutectic solder is formed.

42. A method as recited in claim 37, wherein a number of elements in said solder is increased by at least one element, by said Cu dissolution.

43. A method as recited in claim 37, further comprising annealing at 150 - 250 degrees C for 30 to 60 minutes.

44. A three layer ball limiting structure comprising a Cr adhesion layer for placement on a substrate; a Cu seed layer and a Ni reaction barrier layer on the Cu layer.

45. The structure defined in claim 44, further comprising a lead free solder composition in which the Ni layer is reacted with solder during reflow of the solder.

46. A four layer structure comprising a Cr adhesion layer for deposit on a substrate, a Cu layer on the Cr layer, a Ni reaction barrier layer on said Cu layer, a layer of Cu on top of the Ni layer, said layer of Cu being for dissolving into a lead-free solder to form a binary Sn-Cu alloy or a ternary Sn-Ag-Cu alloy from a plated pure Sn or binary Sn-Ag solder, respectively.